

**What Is Claimed Is:**

1. A device for forming a signature, a predefined number of shift registers being provided, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefinable cycle, a signature being formed in the shift registers after a certain number of data words and cycles,  
wherein a code generator which generates at least one additional bit position in at least one additional shift register from each data word in the signature is also provided.
2. The device as recited in Claim 1,  
wherein the individual shift registers are connected by antivalence points, and the individual bits of the data words at these antivalence points, as well as the at least one additional bit position of the code generator, are inserted to form the signature.
3. The device as recited in Claim 1,  
wherein the individual shift registers are connected by equivalence points, and the individual bits of the data words, as well as the at least one additional bit position of the code generator, are inserted at these equivalence points to form the signature.
4. The device as recited in Claim 1,  
wherein the code generator is designed in such a way that it implements an ECC code and inputs the number of bit positions corresponding to the ECC code being used into a corresponding number of additional shift registers to form the signature.
5. The device as recited in Claim 1,  
wherein the code generator is designed in such a way that it forms a parity bit and inputs it in an additional shift register.
6. The device as recited in Claim 4,  
wherein the code generator is designed in such a way that it implements a Hamming code.
7. The device as recited in Claim 4,  
wherein the code generator is designed in such a way that it implements a Berger code.

8. The device as recited in Claim 4,  
wherein the code generator is designed in such a way that it implements a Bose-Lin  
code.

9. The device as recited in Claim 4,  
wherein the code generator is designed in such a way that it implements a generic  
code generator table.

10. A method for forming a signature, a predefined number of shift registers being  
provided, to which input data to be tested is applied bit-by-bit and in parallel as  
successive data words and which serially shift the input data forward in a  
predefinable cycle, a signature being formed in the shift registers after a certain  
number of data words and cycles,  
wherein a code generator which generates at least one additional bit position in at  
least one additional shift register from each data word in the signature is also  
provided.